REMARKS

Claims 1-21 of the subject patent application are pending, and have been rejected by the Examiner. In the accompanying amendment, claims 1 and 10 have been amended. Support for the accompanying amendment may be found in the specification, in the claims and in the drawings, as originally filed. On account of the foregoing listed support, it is respectfully submitted that these amendments do not add new matter. Moreover, it is respectfully submitted that these amendments place the claims in better form for consideration on appeal, and should be admitted under 37 CFR. 1.116.

Claim Rejections Under 35 U.S.C. § 102

The Examiner has rejected claims 1, 3, 4, 6, 7, 10, 12, 13, 15, 16, 19, and 21 under 35 U.S.C. § 102(e) as being anticipated by Pua et al. (U.S. 2002/0178307). In particular, the Examiner has stated that:

> Pua et al teaches a memory card interface apparatus (adapter 10), system, and method comprising: a plurality of memory card interfaces (30, with at least a subset of the plurality of memory card interfaces configured to interface with a memory card of a first type (Compact Flash, Smart Media, SDIMMC, Memory Stick, etc.), the plurality of memory card interfaces accessible in parallel (the memory card control interface 20 may access the memory card interfaces in parallel); wherein at least one of the memory card interfaces includes an indicator (35) identifying a status of an operation for a respective memory reader interface; wherein the indicator includes a light (the indicator 35 may be an LED) indicating data is being written to a card in the respective memory card interface (the indicators 35 indicate when a card is being accessed); wherein mechanical pins, of at least one of the plurality of memory card interfaces, are inserted directly into a backbone of the apparatus (in that pins of a memory card will connect to pins of the interfaces); wherein a first subset (one of the interfaces 30, for example) of the plurality of memory card interfaces are configured to interface with a memory card of a first type and a second subset (a different one of the interfaces 30, for example) of the plurality of memory card interfaces are configured to interface with a memory card of a second type

> (interfaces are provided for a plurality of types of memory cards, such as Compact Flash, Smart Media, SDIMMC, Memory Stick, etc.), wherein the first and second subset of memory card interfaces are accessible in parallel; a controller circuit (20) and a bus (a high-speed bus) coupled to the controller circuit (see figure 1, paragraphs 22-32, and 37-39).

The Applicants, however, respectfully disagree with the Examiner that rejected claims 1, 3, 4, 6, 7, 10, 12, 13, 15, 16, 19, and 21 are anticipated by Pua.

For example, claim 1 includes the following limitations:

> a plurality of memory card interfaces, with at least a subset of the plurality of memory card interfaces configured to interface with a memory card of a first type, the plurality of memory card interfaces being accessible in parallel.

(Claim 1) (Emphasis Added.)

The above-emphasized limitation of claim 1 requires that the plurality of memory card interfaces be accessible in parallel. The Examiner's above-quoted argument merely shows that the interface 30 for each type of memory card is connected to the memory card control interface 20 in parallel. However, the fact that the interface 30 for each type of memory card is connected to the memory card interface 20 in parallel does not mean that access to the interfaces 30 occurs in parallel.

In fact, Pua describes that the memory card control interface 20 comprises a memory card switching circuit which is switched to one of the interfaces 30 under control of a microprocessor. For example, in paragraph 32, Pua states, "If, for example, the host reads from or writes to a Compact Flash card, the microprocessor will switch this circuit to the Compact Flash interface. If, for example, the host reads from or writes to a Smart Media card, the microprocessor will switch this circuit to the Smart Media interface." Thus, in other words, depending on the type of

card being written to or read from, the microprocessor switches the memory card switching circuit to the interface that supports the card being written to or read from. Since the memory card switching circuit is switched between interfaces, it follows that no more than one interface can be operative at a given point in time. Thus, access to the interfaces does not occur in parallel.

On account of the foregoing, it is respectfully submitted that Pua does not teach or suggest all limitations of claim 1, and that accordingly claim 1 is not anticipated or rendered obvious by Pua.

Given that claims 2-9 depend on claim 1, it is respectfully submitted that these claims are also not anticipated or rendered obvious by Pua.

Independent claims 10 and 19 each have limitations similar to the above-discussed limitations of claim 1, and accordingly, it is respectfully submitted that each of claims 10 and 19 is not anticipated or rendered obvious by Pua.

Given that claims 11-18 and 20-21 depend on claims 10 and 19, respectively, it is respectfully submitted that these claims are also not anticipated or rendered obvious by Pua.

Claim Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 5 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Pua et al. in view of the admitted prior art. Applicants respectfully submit hat the Examiner's rejection of claims 5 and 14 under 35 U.S.C. § 103(a) is now moot by virtue of the above argument that Pua fails to teach or suggest accessing the memory card interfaces in parallel.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,
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